CLOCKED DIODE PULSE AMPLIFIERS FOR MICROWAVE BIT RATES

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Abstract

Diode amplifiers which essentially rely on the storage and switching behavior of step-recovery diodes are investigated for regenerating high bit-rate PCM-type signals. Two preliminary hybrid-integrated versions have been developed and tested at 300 Mbit/s and 1 Gbit/s.

Introduction

Two types of diode pulse amplifier are described which principally appear to be suited for regenerating PCM signals of extremely high bit rates. These amplifiers rely essentially on the minority-carrier storage and reverse switching behavior of step-recovery diodes. The amplifier concepts are related to a low-pulse-rate diode amplifier proposed more than 20 years ago[1] which, however, could not gain any practical importance. But recently it was demonstrated[2] that pulse amplification could be achieved at 250 Mbit/s by using modern step-recovery diodes. Here, we describe investigations on modified circuit designs and on cascading several stages. Amplifiers of the kind discussed might eventually provide an alternative approach in realizing regenerative repeaters for baseband PCM systems such as the high-rate fibre optic system. As shown below, the salient feature of the diode amplifiers is the simultaneous achievement of restoring amplitude, pulse shape, and phase (retiming).

Type 1 Amplifier: Single Stage

Consider the circuit shown in Fig. 1a which contains a Schottky diode SD_1, two step-recovery diodes $SRD_{1,2}$, and a load resistance R_L. An applied input signal pulse charges the diffusion capacitance of SRD_1 via SD_1 and SRD_2, the latter two diodes being both in a low-impedance state because of appropriate bias voltages V_1 to V_3 and a negative sine halfwave of the clock signal (pump) at that instant (Fig. 1b). During the following positive pump halfwave first SRD_2 is discharged and subsequently SRD_1, while SD_1 is in the cut-off state. In this way an output pulse is obtained across R_L, the leading edge being formed by SRD_2, and the trailing edge by SRD_1. The temporal response of the various signals is schematically shown in Fig. 1b.

A single stage can provide a certain amount of voltage and power amplification. In the special case of equal charging and discharging currents through SRD_1 the obtainable voltage gain is given, to first order, by the ratio of output impedance to input impedance, with a limit being set by the available pump power and the resulting output RC time constant. In an experiment with a bybrid-integrated thin-film amplifier at 300 Mbit/s we have measured a voltage gain of somewhat greater than 4 for a load $R_L = 100\ \Omega$. A preliminary experimental result obtained at 1 Gbit/s with $R_L = 100\ \Omega$ is shown in Fig. 3a for a 1100 RZ word pattern, indicating a voltage gain of 2.1. Voltage gain is here defined as the ratio of the voltage difference between minimum 1-bit pulse height and maximum baseline ripple excursion at the output to the corresponding voltage difference of the input signal. The displayed "input signals" are the pulse trains obtained across an ohmic reference resistor R_{ref} (of the specified value) connected directly to the signal generator. Compared to the 300 Mbit/s result, the voltage gain at 1 Gbit/s is distinctly lower. This must attributed mainly to a non-optimum SRD : when the signal charge is injected the diode exhibits at first too high an impedance (conductivity modulation). A remedy would be a diode design of shorter i-layer (<1 μm) and extremely steep adjacent doping profiles. For a comment on the output baseline ripple, particularly the 0-bit signals, see the Conclusions below.

Amplifier Cascade

For achieving substantial power gain several stages must be cascaded in such a way that the stored charge (input current) is increased from stage to stage. Since a single stage provides mainly voltage gain, an impedance transformation must be provided to obtain the necessary current gain for feeding the succeeding stage. This can be effected for instance by employing broadband line transformers of the twisted-pair or symmetric stripline types, such as characterized in Fig. 2. A particular transformer developed has provided an

impedance transformation from 100 ohms to 25 ohms with 3 dB cut-off frequencies of insertion loss at 30 kHz and 3.3 GHz. A thin-film three-stage amplifier cascade using these line transformers has shown a response at 300 Mbit/s as depicted in Fig. 3b. The circuit, which was not yet fully optimized, yielded a charge amplification of about 2.4 and a power gain of approximately 10 dB.

Type 2 Amplifier: Differential Operation

The circuits described so far are not suited for regenerating weak pulses (10 mV range) as they are obtained from the photodiode in a fibre-optic system, for example. For applications of this kind a second amplifier type was developed, namely a differential amplifier containing an extremely broadband 180° magic T as shown schematically in Fig. 4. Step-recovery diodes SRD_S, SRD_R are connected to one pair of opposite ports, whereas a sinusoidal pump generator (clock) and the load terminate the other pair of ports. By applying appropriate bias voltages and the positive pump halfwave to the diodes they are first supplied with the same basic charge. A signal pulse applied to only SRD_S then causes a slight charge difference. As a result SRD_S switches somewhat later from the low-impedance to the high-impedance state, during the subsequent negative pump halfwave, than SRD_R does. As long as the SRD impedances are unequal, energy is transferred from the pump to the load. In this way SRD_R forms the leading edge, and SRD_S the trailing edge, of the generated output pulse. In the actual circuit an additional Schottky diode each was connected across the signal and reference ports for providing a low-impedance path during the charging interval.

For the experiments a particular magic T was developed being, in fact, a six-port coaxial/stripline version with "lumped" branching point (avoidance of resonant structures). Broadband matching from approximately 100 kHz to 10 GHz was obtained. Besides two pump ports, the T possesses two output ports delivering identical signals, but of opposite polarity. Fig. 5 shows pulse trains measured (output signal across one port) on a single stage at 300 Mbit/s (1100 pattern) and 1 Gbit/s (111000 pattern). The voltage gain is 3.35 and 3.4, respectively. The gain should improve, for instance, by using step-recovery diodes of shorter switching time. With the 300 Mbit/s version amplification of pulses having peak pulse amplitudes as low as 2 mV could be achieved, though the circuit is not restricted to low-level operation as can be seen from Fig. 5b. In the 1 Gbit/s experiment R_L was increased to the highest value (1050 Ω) which still brought an increase in voltage gain at the fixed pump voltage amplitude of 540 mV. The input signal in Fig. 5b shows a tendency towards an NRZ pattern; the inherent amplifier action turns this into a definite RZ signal at the output.

It is intended also to cascade differential amplifiers. In this case the two output ports of the amplifier will be connected, via an impedance transformer, to the SRD_S port and the SRD_R port, respectively, of the following stage, thereby making use of the full output. Since line transformers are limited to fairly low transformation ration, we consider as well employing field-effect transistor coupling, in order to fully utilize the voltage amplification each preceding stage can deliver (high output impedance); transistor coupling might be useful also for cascading type 1 amplifiers.

Conclusions

Diode amplifiers of the kind described require a sinusoidal pump signal which is available as clock signal in the applications anvisaged. It has principally been shown that the amplifiers operate rather satisfactorily at rates of 300 Mbit/s; certain improvements will still be possible. At 1 Gbit/s, though pulse amplification has been achieved, more distinct advancements are required. Besides optimizing SRD parameters for this particular application as stated above, the diodes should possess a smaller area for reduced depletion-layer capacitance (which also shortens switching time). This capacitance is mainly responsible for the unwanted 0-bit signals of the type 1 amplifier (Fig. 3). In the type 2 amplifier, on the other hand, the 0-bit response (Fig. 5) is to first degree caused by the pump-controlled switching process of the Schottky diodes across the signal and reference ports. Thus, also improved Schottky-diode design (e.g. very small series resistance) and diode-pair matching are called for. It should be pointed out that both types of amplifier only scarcely respond to baseline ripple as long as its mean value over the charging interval approaches zero since the amplifier integrates the charge received. Improvements are, finally, intended by employing chip diodes instead of the so far used LID mounted diodes and by further advancing the circuit lay-out, particulary with regard to the avoidance of unsymmetries etc.

Acknowledgements

Financial support provided by the German Research Council (DFG) is gratefully acknowledged. Furthermore we would like to thank Siemens AG and Hewlett-Packard Co. for providing diodes.

References

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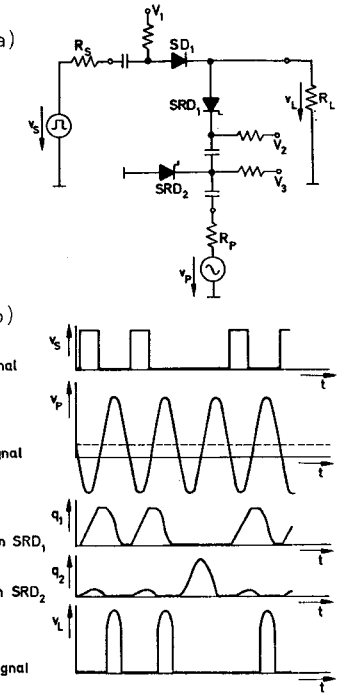

Fig. 1

Basic circuit (a) and principal pulse response (b) of type 1 amplifier

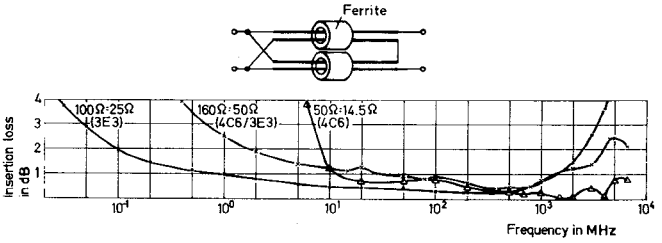

Fig. 2 Measured performance of several line transformers

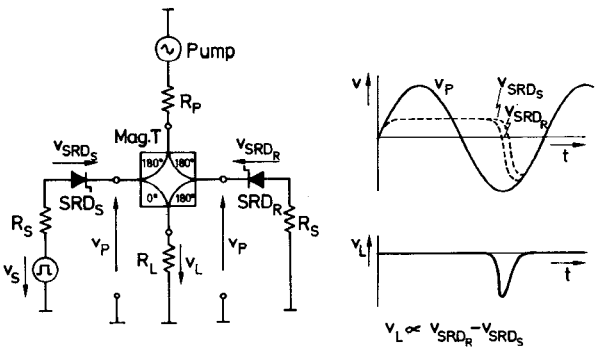

Fig. 4 Basic circuit and principal pulse behavior of type 2 amplifier

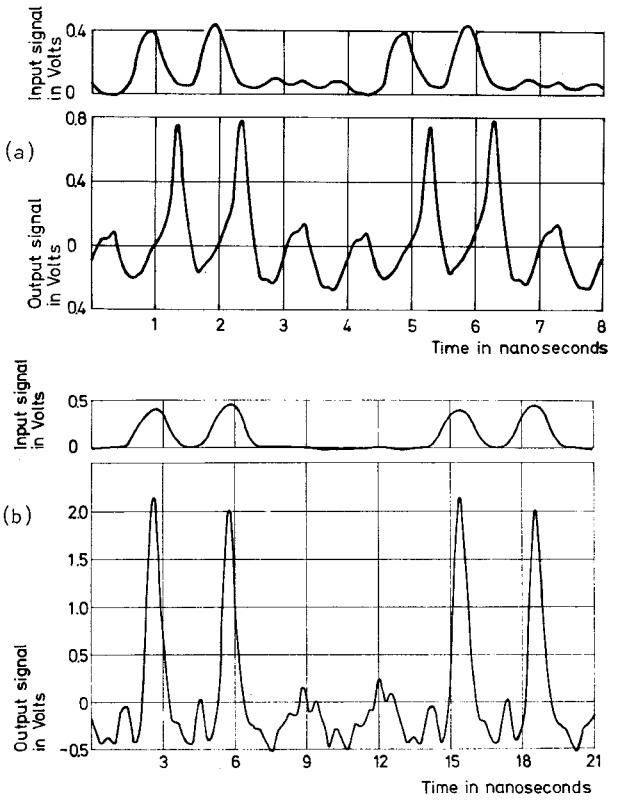

Fig. 3 Measured pulse response of type 1 amplifier; (a) 1 Gbit/s, single stage, R_L = 100 Ω, R_{ref} = 50 Ω; (b) 300 Mbit/s, 3-stage cascade, $R_L = R_{ref}$ = 25 Ω

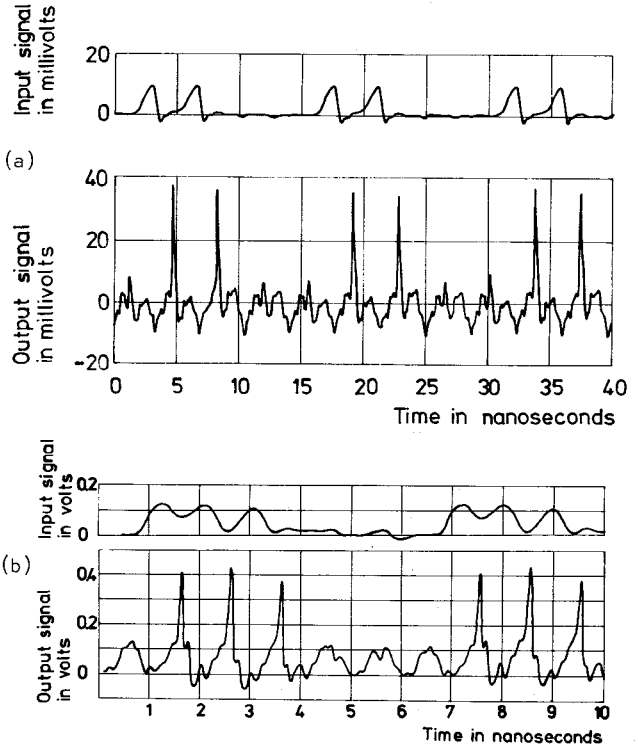

Fig. 5 Measured pulse response of type 2 amplifier, single stage, (a) 300 Mbit/s, $R_L = R_{ref}$ = 50 Ω; (b) 1 Gbit/s, R_L = 1050 Ω, R_{ref} = 50 Ω